WHAT IS CLAIMED IS:

1. A method of making an electrical device, comprising:

(A) depositing a plurality of nanowires onto a substrate in a thin film; and

(B) forming first and second electrical contacts on the substrate;

wherein at least one of the nanowires of the thin film couples the first electrical contact to the second electrical contact.

2. The method of claim 1, wherein the plurality of nanowires comprises a plurality of thermoelectric nanowires, wherein step (A) comprises:

depositing the plurality of thermoelectric nanowires onto the substrate in a thin film of thermoelectric nanowires;

whereby the electrical device exhibits thermoelectric characteristics during operation.

3. The method of claim 1, wherein the plurality of nanowires comprises a plurality of piezoelectric nanowires, wherein step (A) comprises:

depositing the plurality of piezoelectric nanowires onto the substrate in a thin film of piezoelectric nanowires;

whereby the electrical device exhibits piezoelectric characteristics during operation.

4. The method of claim 1, wherein the plurality of nanowires comprises a plurality of magnetic nanowires, wherein step (A) comprises:

depositing the plurality of magnetic nanowires onto the substrate in a thin film of magnetic nanowires;

whereby the electrical device exhibits magnetic characteristics during operation.

5. The method of claim 1, wherein the plurality of nanowires comprises a plurality of ferroelectric nanowires, wherein step (A) comprises:

depositing the plurality of ferroelectric nanowires onto the substrate in a thin film of ferroelectric nanowires;

whereby the electrical device exhibits ferroelectric characteristics during operation.

6. The method of claim 1, wherein the plurality of nanowires comprises a plurality of metallic nanowires, wherein step (A) comprises:

depositing the plurality of metallic nanowires onto the substrate in a thin film of metallic nanowires.

7. The method of claim 1, wherein the plurality of nanowires comprises a plurality of transition metal oxide nanowires, wherein step (A) comprises:

depositing the plurality of transition metal oxide nanowires onto the substrate in a thin film of transition metal oxide nanowires.

8. The method of claim 1, wherein step (B) comprises:

forming the first and second electrical contacts on at least a portion of the plurality of nanowires on the substrate.

9. The method of claim 1, wherein step (A) comprises:

depositing the plurality of nanowires onto the substrate after forming the first and second electrical contacts on the substrate in step (B).

10. The method of claim 1, wherein the first electrical contact is a source electrode, and the second electrical contact is a drain electrode, wherein step (B) comprises:

forming the source and drain electrodes on the substrate

11. The method of claim 10, further comprising:

(C) forming a gate electrode on the substrate.

12. The method of claim 11, wherein step (C) comprises:

forming the gate electrode on at least a portion of the plurality of nanowires on the substrate.

13. The method of claim 11, wherein step (A) comprises:

depositing the plurality of nanowires onto the substrate after forming the gate electrode on the substrate in step (C).

14. The method of claim 1, wherein the first electrical contact is a cathode electrode, and the second electrical contact is an anode electrode, wherein step (B) comprises:

forming the cathode and anode electrodes on the substrate.

15. The method of claim 1, wherein step (A) comprises:

depositing the plurality of nanowires onto the substrate such that the nanowires are randomly aligned with respect to their long axes.

16. The method of claim 1, further comprising:

(E) aligning the nanowires so that their long axes are substantially parallel.

17. An electronic substrate having a plurality of electrical devices, comprising:

a substrate;

a thin film of nanowires formed on said substrate, wherein said thin film of nanowires defines a plurality of semiconductor device regions; and

a plurality of contact pairs formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein each contact pair has at least one nanowire of the thin film of nanowires coupled therebetween.

18. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of thermoelectric nanowires.

19. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of piezoelectric nanowires.

20. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of magnetic nanowires.

21. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of ferroelectric nanowires.

22. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of metallic nanowires.

23. The electronic substrate of claim 17, wherein the thin film of nanowires comprises a plurality of transition metal oxide nanowires.

24. The electronic substrate of claim 17, wherein the contact pairs are formed on at least a portion of the plurality of nanowires on the substrate.

25. The electronic substrate of claim 17, wherein the thin film of nanowires is formed on the substrate after forming the plurality of contact pairs on the substrate.

26. The electronic substrate of claim 17, wherein each contact pair includes a source electrode and a drain electrode.

27. The electronic substrate of claim 26, wherein a gate electrode is formed on the substrate corresponding to each contact pair.

28. The electronic substrate of claim 27, wherein the gate electrode is formed on the thin film of nanowires.

29. The electronic substrate of claim 27, wherein the thin film of nanowires is formed on the substrate after forming the gate electrode on the substrate.

30. The electronic substrate of claim 17, wherein each contact pair includes a cathode electrode and an anode electrode.

31. The electronic substrate of claim 17, wherein the nanowires of the thin film of nanowires are randomly aligned with respect to each other.

32. The electronic substrate of claim 17, wherein the nanowires of the thin film of nanowires are aligned so that their long axes are substantially parallel.

33. A method of making a thin film for use in one or more semiconductor devices, comprising:

(A) forming a first plurality of nanowires that are p-doped;

(B) forming a second plurality of nanowires that are n-doped; and

(C) depositing the first plurality of nanowires and second plurality of nanowires onto a substrate to form a thin film of nanowires that includes n-doped and p-doped nanowires;

whereby the thin film of nanowires exhibits characteristics of both n-doped and p-doped nanowires.

34. The method of claim 33, further comprising:

(D) allowing the mixture of n-doped and p-doped nanowires to become immobilized on the substrate.

35. The method of claim 34, further comprising:

(E) forming at least first and second electrical contacts in predetermined regions of the substrate;

wherein step (D) comprises allowing the n-doped and p-doped nanowires to immobilize in contact with each of the at least first and second electrical contacts.

36. The method of claim 33, wherein step (C) comprises:

(1) depositing the first plurality of nanowires on a first region of the substrate; and

(2) depositing the second plurality of nanowires on a second region of the substrate;

wherein the thin film of nanowires includes regionally segregated n-doped and p-doped nanowires on the substrate.

37. The method of claim 33, wherein step (C) comprises:

(1) depositing the first plurality of nanowires on the substrate to form a first sublayer of the thin film of nanowires; and

(2) depositing the second plurality of nanowires on the first sublayer to form a second sublayer of the thin film of nanowires on the first sublayer.

38. The method of claim 33, wherein step (C) comprises:

(1) depositing the second plurality of nanowires on the substrate to form a first sublayer of the thin film of nanowires; and

(2) depositing the first plurality of nanowires on the first sublayer to form a second sublayer of the thin film of nanowires on the first sublayer.

39. The method of claim 33, wherein step (C) comprises:

mixing the first plurality of nanowires and the second plurality of nanowires; and

depositing the mixed first plurality and second plurality of nanowires onto the substrate to form the thin film of nanowires.

40. The method of claim 33, wherein said steps (A) and (B) each comprise:

doping a core of the nanowires.

41. The method of claim 33, wherein said steps (A) and (B) each comprise:

doping a shell of the nanowires.

42. The method of claim 33, wherein said steps (A) and (B) each comprise:

doping a core and a shell of the nanowires.

43. A semiconductor device having operational characteristics of n- and p-doped materials, comprising:

a substrate;

a plurality of electrical contacts formed on the substrate; and

a thin film of n-doped nanowires and p-doped nanowires adhering to the substrate in contact with each of the plurality of electrical contacts.

44. The semiconductor device of claim 43, wherein the thin film of n-doped and p-doped nanowires comprises:

a first region that includes a plurality of n-doped nanowires adhering to the substrate; and

a second region that includes a plurality of p-doped nanowires adhering to the substrate;

wherein the first region and second region are substantially non-overlapping.

45. The semiconductor device of claim 43, wherein the thin film of n-doped and p-doped nanowires comprises:

a first sublayer that includes a plurality of n-doped nanowires; and

a second sublayer that includes a plurality of p-doped nanowires.

46. The semiconductor device of claim 43, wherein the thin film of n-doped and p-doped nanowires comprises:

a mixture of n-doped nanowires and p-doped nanowires.

47. A method of making an electrical device, comprising:

(A) forming a plurality of nanowires so that each nanowire has along its long axis at least one first portion doped with a first dopant and at least one second portion doped with a second dopant, each nanowire having a spacing between consecutive junctions of the first and second portions substantially equal to a first distance;

(B) forming a pair of electrical contacts on the substrate, wherein a distance between the electrical contacts is approximately equal to the first distance; and

(C) depositing the plurality of nanowires onto the substrate, wherein at least one nanowire of the plurality of nanowires couples the first electrical contact to the second electrical contact.

48. The method of claim 47, wherein step (A) comprises:

growing each nanowire, wherein said growing step comprises:

(1) forming an alternating pattern of the doped first portions and the doped second portions along the long axis of each nanowire.

49. The method of claim 48, wherein step (1) comprises:

alternately supplying a first nanowire source material that comprises the first dopant and a second nanowire source material that comprises the second dopant.

50. The method of claim 47, wherein step (A) comprises:

growing each nanowire; and

doping each grown nanowire to have alternating doped first portions and doped second portions along its long axis.

51. A method of making an electrical device on a substrate, comprising:

(A) forming a plurality of nanowires so that each nanowire has a plurality of repeating patterns of doped portions along its long axis, each pattern of the repeating patterns having a length substantially equal to a first distance;

(B) forming a plurality of electrical contacts on the substrate, wherein a distance between a pair of electrical contacts of the plurality of electrical contacts is approximately equal to the first distance;

(C) depositing the plurality of nanowires onto the substrate, wherein the plurality of nanowires adhere to the plurality of electrical contacts.

52. The method of claim 51, wherein step (A) comprises:

(1) growing each nanowire to include the plurality of repeating patterns of doped portions in series along its long axis.

53. The method of claim 52, wherein step (1) comprises:

(i) growing each nanowire according to a first pattern, wherein the first pattern comprises a first portion and a second portion in series, wherein the first portion includes a first dopant and the second portion includes a second dopant; and

(ii) repeating step (i) at least once to repeat the first pattern along the long axis of each nanowire.

54. The method of claim 52, wherein step (1) comprises:

(i) growing each nanowire according to a first pattern, wherein the first pattern comprises a first portion, a second portion, and a third portion in series, wherein the first and third portions include a first dopant; and

(ii) repeating step (i) at least once to repeat the first pattern along the long axis of each nanowire.

55. The method of claim 54, wherein step (i) comprises:

growing the second portion to include a second dopant.

56. The method of claim 54, wherein step (i) comprises:

growing the second portion to be intrinsic.

57. The method of claim 51, wherein step (A) comprises:

growing each nanowire; and

doping each grown nanowire to have the repeating pattern of doped portions along its long axis.

58. The method of claim 57, wherein step (1) comprises:

(i) doping each grown nanowire according to a first pattern, wherein the first pattern comprises a first portion and a second portion in series, wherein the first portion includes a first dopant and the second portion includes a second dopant; and

(ii) repeating step (i) at least once to repeat the first pattern along the long axis of each grown nanowire.

59. The method of claim 57, wherein step (1) comprises:

(i) doping each grown nanowire according to a first pattern, wherein the first pattern comprises a first portion, a second portion, and a third portion in series, wherein the first and third portions include a first dopant; and

(ii) repeating step (i) at least once to repeat the first pattern along the long axis of each grown nanowire.

60. The method of claim 59, wherein step (i) comprises:

doping the second portion with a second dopant.

61. The method of claim 59, wherein step (i) comprises:

allowing the second portion to be intrinsic.

62. The method of claim 51, wherein the plurality of electrical contacts include anode and cathode electrodes, wherein step (B) comprises:

forming the anode and cathode electrodes on the substrate to have a distance therebetween approximately equal to the first distance.

63. The method of claim 51, wherein the plurality of electrical contacts include a drain electrode, a gate electrode, and a source electrode, wherein step (B) comprises:

forming the drain electrode and gate electrode on the substrate to have a distance therebetween approximately equal to the first distance; and

forming the source electrode on the substrate to have a distance between the source electrode and gate electrode approximately equal to the first distance.

64. An electrical device, comprising:

a substrate;

first and second electrical contacts formed on said substrate; and

a plurality of nanowires, wherein each nanowire has an alternating pattern of p-doped portions and n-doped portions along its long axis, each nanowire having a spacing between consecutive junctions of said p-doped portions and said n-doped portions substantially equal to a first distance, wherein at least one of the nanowires couples said first electrical contact to said second electrical contact;

wherein a distance between said first electrical contact and said second electrical contact is approximately equal to said first distance.

65. The device of claim 64, wherein said first electrical contact is a source electrode, and said second electrical contact is a gate electrode, further comprising:

a source electrode formed on said substrate, wherein a distance between the source electrode and gate electrode is approximately equal to said first distance.

66. The device of claim 64, wherein said first electrical contact is a cathode electrode, and said second electrical contact is an anode electrode.

67. A method of making a light emitting thin film, comprising:

(A) selecting at least one light emitting semiconductor nanowire material;

(B) forming a plurality of nanowires from the selected at least one light emitting semiconductor nanowire material;

(C) doping each nanowire so that each nanowire includes at least one P-N junction; and

(D) depositing the plurality of nanowires onto a substrate.

68. The method of claim 67, further comprising:

(E) forming a first electrical contact and a second electrical contact on the substrate, wherein at least one of the nanowires couples the first electrical contact to the second electrical contact.

69. The method of claim 68, wherein step (D) is performed before step (E).

70. The method of claim 68, wherein step (E) comprises:

forming the first and second electrical contacts on at least a portion of the plurality of nanowires on the substrate.

71. The method of claim 68, wherein the first electrical contact is a source electrode and the second electrical contact is a drain electrode, further comprising:

(F) forming a gate electrode on the substrate.

72. The method of claim 68, wherein the first electrical contact is a cathode electrode and the second electrical contact is an anode electrode, wherein step (E) comprises:

(F) forming the cathode electrode and anode electrode on the substrate.

73. The method of claim 67, wherein step (C) comprises:

doping each nanowire to have alternating N- and P- doped portions, each nanowire having a spacing between consecutive junctions of alternately doped portions substantially equal to a first distance.

74. The method of claim 73, further comprising:

(E) forming a first electrical contact and a second electrical contact on the substrate, wherein at least one of the nanowires couples the first electrical contact to the second electrical contact, wherein a distance between

the first and second electrical contacts is approximately equal to the first distance.

75. The method of claim 67, wherein the at least one light emitting semiconductor material selected in step (A) includes at least one of a fluorescent, phosphorescent, electroluminescent, and cathodoluminescent material, wherein step (B) comprises:

forming a plurality of nanowires from the selected at least one of a fluorescent, phosphorescent, electroluminescent, and cathodoluminescent material.

76. The method of claim 67, wherein the at least one light emitting semiconductor material selected in step (A) includes a plurality of fluorescent materials, wherein step (B) comprises:

forming a plurality of nanowires from the selected plurality of fluorescent materials.

77. The method of claim 67, wherein step (B) comprises:

forming the plurality of nanowires so that each nanowire has substantially the same diameter.

78. The method of claim 67, wherein step (B) comprises:

forming the plurality of nanowires to include nanowires having a plurality of diameters.

79. The method of claim 67, wherein step (A) comprises:

(1) selecting a plurality of light emitting semiconductor nanowire materials such that each selected light emitting semiconductor nanowire material emits a color of light different from others of the selected light emitting semiconductor nanowire materials.

80. The method of claim 79, wherein step (1) comprises:

selecting the plurality of light emitting semiconductor nanowire materials so that white light is emitted by the thin film.

81. The method of claim 67, wherein step (A) comprises:

selecting the at least one light emitting semiconductor nanowire material so that pink, red, orange, yellow, green, blue, purple, indigo, violet, brown, infrared, near infrared, or ultraviolet light is emitted by the thin film.

82. The method of claim 67, wherein step (D) is performed before step (C).

83. The method of claim 67, wherein step (C) is performed before step (D).

84. A method of making a light emitting semiconductor device, comprising:

(A) selecting at least one light emitting semiconductor nanowire material;

(B) forming a plurality of nanowires from the selected at least one light emitting semiconductor nanowire material;

(D) depositing the plurality of nanowires onto a substrate; and

(E) forming a first electrical contact and a second electrical contact on the substrate, wherein at least one of the nanowires couples the first electrical contact to the second electrical contact;

wherein during operation of the device, light is emitted from a junction of the nanowires and one of the first and second electrical contacts.

85. The method of claim 84, wherein a Schotky diode is formed by the coupling of at least one of the nanowires to one of the first and second electrical contacts.

86. A light emitting semiconductor device, comprising:

a substrate;

first and second electrical contacts formed on said substrate; and

a plurality of nanowires that each comprise at least one light emitting semiconductor nanowire material, wherein at least one of the nanowires couples the first electrical contact to the second electrical contact;

wherein said plurality of nanowires are immobilized on said substrate in contact with both electrical contacts.

87. The device of claim 86, wherein during operation of the device, light is emitted from a junction of the nanowires and one of the first and second electrical contacts.

88. The device of claim 86, wherein each nanowire is doped to include a p-n junction.

89. The device of claim 86, wherein a distance between said pair of electrical contacts is approximately equal to a first length;

wherein each nanowire is doped to have a plurality of p-n junctions along its respective long axis, each nanowire having a spacing between adjacent p-n junctions approximately equal to said first length.

90. The device of claim 86, wherein said each nanowire comprises a fluorescent nanowire material.

91. The device of claim 90, wherein said fluorescent nanowire material includes GaN.

92. The device of claim 90, wherein said fluorescent nanowire material includes at least one of CdSe, InP, InAs, CdS, CdTe, ZnS, ZnSe, ZnO, PbSe, PbTe, PbS, HgTe, HgSe, and HgS.

93. The device of claim 86, wherein said plurality of nanowires comprises a plurality of fluorescent nanowire materials.

94. The device of claim 86, wherein all nanowires of said plurality of nanowires have substantially the same diameter.

95. The device of claim 86, wherein said plurality of nanowires includes nanowires having a plurality of diameters.

96. The device of claim 86, wherein the semiconductor device emits pink, red, orange, yellow, green, blue, purple, indigo, violet, brown, infrared, near-infrared, or ultraviolet light during operation.

97. The device of claim 86, wherein the semiconductor device emits white light during operation.

98. A method for positioning nanowires on a target surface, comprising:

(A) mating a first surface of a flow mask with the target surface such that at least one channel formed in the first surface of the flow mask covers a portion of the target surface;

(B) flowing a liquid that contains a plurality of nanowires through the at least one channel; and

(C) permitting nanowires contained in the liquid flowing through the at least one channel to become positioned on the portion of the target surface covered by the at least one channel.

99. The method of claim 98, further comprising:

(D) discontinuing the flow of the liquid through the at least one channel to allow nanowires to remain positioned on the portion of the target surface.

100. The method of claim 98, wherein the at least one channel comprises a plurality of channels formed in the first surface, wherein step (B) comprises:

flowing a liquid that contains a plurality of nanowires through the plurality of channels.

101. The method of claim 100, wherein each channel of the plurality of channels covers a corresponding portion of the target surface, wherein step (C) comprises:

permitting nanowires contained in the liquid flowing through the plurality of channels to become positioned on the corresponding portion of the target surface covered by each channel of the plurality of channels.

102. The method of claim 98, wherein the target surface has a plurality of electrically conductive features formed thereon, wherein step (C) comprises:

forming at least one connection between electrically conductive features of the plurality of electrically conductive features with at least one nanowire.

103. The method of claim 98, wherein step (B) comprises:

causing nanowires positioned on the portion of the target surface to be oriented substantially parallel to a direction of flow of the liquid through the at least one channel.

104. The method of claim 98, further comprising:

(D) selecting a density of nanowires in the liquid.

105. The method of claim 104, wherein step (D) comprises:

selecting the density of nanowires in the liquid so that a sufficient number of nanowires are permitted in step (C) to become positioned on the covered portion of the target surface to form electrical connections on the covered portion of the target surface.

106. An apparatus for positioning nanowires on a target surface, comprising:

a body having a first surface configured to mate with the target surface;

at least one channel formed in said first surface;

an input port formed in said body to supply a flow of nanowires to said at least one channel; and

an output port formed in said body to remove the flow of nanowires from said at least one channel;

wherein said at least one channel is formed to allow nanowires of said flow of nanowires to be positioned on a portion of the target surface covered by said at least one channel when said first surface of said body mates with the target surface.

107. The apparatus of claim 106, wherein said at least one channel comprises a plurality of channels formed in said first surface.

108. The apparatus of claim 106, wherein said target surface is a semiconductor wafer surface.

109. The apparatus of claim 108, wherein said semiconductor wafer surface includes an array of integrated circuits formed thereon.

110. The apparatus of claim 106, wherein said target surface is a substrate surface.

111. The apparatus of claim 106, wherein said flow of nanowires comprises a liquid containing a plurality of nanowires.

112. The apparatus of claim 106, wherein the target surface has a plurality of electrically conductive traces formed thereon, wherein said at least one channel allows nanowires of said flow of nanowires to form at least one connection between electrically conductive traces of said plurality of electrically conductive traces.

113. The apparatus of claim 106, wherein said nanowires positioned on the portion of the target surface are oriented substantially parallel to a direction of flow through said at least one channel.

114. The apparatus of claim 106, wherein a channel width of said at least one channel is in the range of 1 μm to 1000 μm.

115. A system for applying nanowires to a target surface, comprising:

a solution source that provides a nanowire solution, wherein said nanowire solution comprises a liquid containing a plurality of nanowires; and

a nozzle coupled to said solution source, wherein said nozzle has at least one output opening;

wherein said nozzle directs the nanowire solution through said at least one output opening onto the target surface, said nanowires of said nanowire solution being directed onto the target surface to be aligned on said target surface substantially parallel to each other.

116. The system of claim 115, wherein said nozzle has a plurality of output openings.

117. The system of claim 116, wherein said plurality of output openings apply the nanowire solution to overlapping portions of the target surface.

118. The system of claim 116, wherein said plurality of output openings apply the nanowire solution to a plurality of non-overlapping portions of the target surface.

119. The system of claim 115, wherein a width of an output opening of said at least one output opening is in a range of 1 μm to 1000 μm.

120. The system of claim 115, wherein a width of an output opening of said at least one output opening is greater than or equal to (≥) a length of a nanowire of said plurality of nanowires.

121. A method for applying nanowires to a target surface substantially in alignment, comprising:

(A) providing a nanowire solution, wherein the nanowire solution comprises a liquid containing a plurality of nanowires; and

(B) directing the nanowire solution through at least one output opening of a nozzle onto the target surface;

wherein step (B) includes the step of causing the nanowires to be substantially aligned parallel to each other on the target surface.

122. The method of claim 121, wherein step (B) further comprises:

directing the nanowire solution to overlapping portions of the target surface.

123. The method of claim 121, wherein step (B) further comprises:

directing the nanowire solution to a plurality of non-overlapping portions of the target surface.

124. The method of claim 121, wherein step (B) further comprises:

applying pressure to force the nanowire solution through the at least one output opening of the nozzle onto the target surface.

125. The method of claim 121, wherein the target surface is a substrate, wherein step (B) further comprises:

directing the nanowire solution through the at least one output opening of the nozzle onto the substrate.

126. The method of claim 121, wherein the target surface is a wafer, wherein step (B) further comprises:

directing the nanowire solution through the at least one output opening of the nozzle onto the wafer.

127. The method of claim 121, wherein the target surface is a substantially continuous sheet, wherein step (B) further comprises:

directing the nanowire solution through at least one output opening of a nozzle onto the sheet;

wherein the method further comprises:

(C) adjusting the position of the sheet relative to the nozzle.

128. The method of claim 121, further comprising:

(C) causing the nanowires to become attached to the target surface.

129. The method of claim 128, wherein step (C) comprises:

curing the nanowire solution on the target surface.

130. The method of claim 121, wherein step (C) comprises:

applying a charge to the target surface.

131. A method of making a large area, macro electronic substrate having a plurality of semiconductor devices, comprising:

(A) directing a nanowire solution through at least one output opening of a nozzle onto a substrate to form a thin film of nanowires with a sufficient density of nanowires to achieve an operational current density;

(B) patterning the thin film of nanowires to define a plurality of semiconductor device regions; and

(C) forming ohmic contacts at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices.

132. The method of claim 131, wherein step (A) comprises:

causing the nanowires of the thin film of nanowires to be substantially aligned.

133. The method of claim 131, further comprising:

(D) curing the thin film of nanowires.

134. The method of claim 131, further comprising:

(D) applying a charge to the target surface.

135. A method of designing conducting nanowires having high mobility of electrons, comprising:

(A) selecting a semiconductor material; and

(B) determining a maximum diameter for a nanowire made from the selected semiconductor material that provides substantial quantum confinement of electrons.

136. The method of claim 135, wherein step (B) comprises:

calculating the maximum diameter as follows:

$$\text{the maximum diameter} = \sqrt{\frac{Nk_bT(8.9)\hbar^2}{2m_{eff}}}$$

wherein:

$\hbar$ = Planck's constant ÷ 2π

= 6.626×10^{-34} J-sec ÷ (2×3.1416)

(or 4.14×10^{-15} eV-sec ÷ 2×3.1416);

= 1.0545×10^{-34} J-sec (6.589×10^{-16} eV-sec)

m_{eff} = effective mass of the selected semiconductor material;

N = a predetermined factor;

k_b = Boltzmann's constant = 8.62×10^{-5} eV/°K; and

T = operating temperature;

wherein at room temperature, k_bT = .0259 eV.

137. The method of claim 135, comprising:

(C) forming a plurality of nanowires from the selected semiconductor material, each nanowire of the plurality of nanowires being formed to have a diameter less than or equal to (≤) to the determined maximum diameter.

138. The method of claim 135, wherein step (1) comprises:

selecting the semiconductor material to be one of Si, Ge, AlN, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb, ZnO, and ZnS.

139. The method of claim 135, wherein step (C) comprises:

forming each nanowire of the plurality of nanowires to have a predetermined length, wherein each nanowire allows for ballistic transport of electrons through the nanowire.

140. The method of claim 136, wherein the predetermined factor, *N*, is greater than or equal (≥) to 3.

141. The method of claim 140, wherein the predetermined factor, *N*, is greater than or equal (≥) to 5.

142. A method of fabricating conducting nanowires having high mobility of electrons, comprising:

(A) selecting a semiconductor material; and

(B) forming a plurality of nanowires from the selected semiconductor material, wherein each nanowire is formed to have a diameter

less than or equal to (≤) a maximum diameter determined for the selected semiconductor material to allow each nanowire to retain substantial quantum confinement of electrons.

143. The method of claim 142, wherein step (B) comprises:

calculating the maximum diameter as follows:

$$\text{the maximum radius} = \sqrt{\frac{(8.9)\hbar^2}{2m_{eff}Nk_bT}}$$

wherein:

$\hbar$ = Planck's constant ÷ 2π

= 6.626×10^{-34} J-sec ÷ (2 × 3.1416)

(or 4.14×10^{-15} eV-sec ÷ 2 × 3.1416)

= 1.0545×10^{-34} J-sec (6.589×10^{-16} eV-sec);

m_{eff} = effective mass of the semiconductor material;

N = a predetermined factor;

k_b = Boltzmann's constant = 1.38×10^{-23} J/°K (8.62×10^{-5} eV/°K); and

T = operating temperature;

wherein at room temperature, $k_bT = 4.144 \times 10^{-21}$ J (.0259 eV).

144. The method of claim 142, wherein step (1) comprises:

selecting the semiconductor material to be one of Si, Ge, AlN, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb, ZnO, and ZnS.

145. The method of claim 142, wherein each nanowire has a length less than or equal to (≤) a predetermined length such that ballistic transport of electrons can occur through the nanowire.

146. The method of claim 143, wherein the predetermined factor, *N*, is greater than or equal (≥) to 3.

147. The method of claim 146, wherein the predetermined factor, *N*, is greater than or equal (≥) to 5.

148. The method of claim 142, further comprising:

(C) configuring the plurality of nanowires to use electrons as conducting carriers, whereby a phonon scattering of electrons is reduced in the nanowires of the plurality of nanowires.

149 The method of claim 148, wherein step (C) comprises:

(1) doping the plurality of nanowires with an n-type dopant material.

150 The method of claim 148 wherein step (C) comprises:

(1) doping the plurality of nanowires with a p-type dopant material; and

(2) operating the plurality of nanowires in an inversion mode by applying a sufficient bias voltage to the plurality of nanowires to cause electrons to be conducting carriers.

151. The method of claim 150, wherein the plurality of nanowires are coupled between source and drain electrodes of a transistor, wherein step (2) comprises:

applying the bias voltage to the plurality of nanowires as a gate bias voltage for the transistor.

152. A conductor having a high mobility of electrons, comprising:

a thin film of nanowires having a sufficient density of nanowires to achieve an operational current level, each nanowire comprising a semiconductor material and having a diameter less than or equal to ($\leq$) a maximum diameter determined for said semiconductor material to allow said each nanowire to retain substantial quantum confinement of electrons.

153. The conductor of claim 152, wherein said maximum diameter is calculated according to:

$$\text{the maximum radius} = \sqrt{\frac{(8.9)\hbar^2}{2m_{eff}Nk_bT}}$$

wherein:

$\hbar$ = Planck's constant $\div 2\pi$

$= 6.626 \times 10^{-34}$ J-sec $\div (2 \times 3.1416)$

(or 4.14×10^{-15} eV-sec $\div 2 \times 3.1416$)

$= 1.0545 \times 10^{-34}$ J-sec (6.589×10^{-16} eV-sec);

m_{eff} = effective mass of the semiconductor material;

N = a predetermined factor;

k_b = Boltzmann's constant = 1.38×10^{-23} J/°K (8.62×10^{-5} eV/°K); and

T = operating temperature;

wherein at room temperature, $k_bT = 4.144\text{x}10^{-21}$ J (.0259 eV).

154. The conductor of claim 152, wherein said semiconductor material is one of Si, Ge, AlN, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb, ZnO, and ZnS.

155. The conductor of claim 152, wherein said each nanowire has a length less than or equal to (≤) a predetermined length such that ballistic transport of electrons can occur through said each nanowire.

156. The conductor of claim 153, wherein the predetermined factor, N, is greater than or equal (≥) to 3.

157. The conductor of claim 156, wherein the predetermined factor, N, is greater than or equal (≥) to 5.

158. The conductor of claim 152, wherein the nanowires are configured to use electrons as conducting carriers, whereby a phonon scattering of electrons is reduced in the nanowires.

159. The conductor of claim 158, wherein the nanowires are doped with an n-type dopant material to be configured to use electrons as conducting carriers.

160. The conductor of claim 158, wherein the nanowires are doped with an p-type dopant material, and

wherein the thin film of nanowires are operated in an inversion mode by applying a sufficient bias voltage to the thin film of nanowires so that electrons are used as conducting carriers.

161. The conductor of claim 160, wherein the plurality of nanowires are coupled between source and drain electrodes of a transistor, wherein the bias voltage is applied to the plurality of nanowires as a gate bias voltage for the transistor.

162. A method of fabricating nanowires having reduced surface scattering, comprising:

(A) selecting a semiconductor material;

(B) forming a plurality of nanowires from the selected semiconductor material; and

(C) coating a circumferential surface of each nanowire of the plurality of nanowires with an insulating layer.

163. The method of claim 162, wherein the insulating layer comprises a dielectric material, wherein step (C) comprises:

coating each nanowire of the plurality of nanowires with the dielectric material.

164. The method of claim 162, wherein the insulating layer comprises an oxide, wherein step (C) comprises:

oxidizing each nanowire of the plurality of nanowires to create a plurality of oxidized nanowires.

165. The method of claim 164, further comprising:

(D) annealing each oxidized nanowire of the plurality of oxidized nanowires.

166. The method of claim 165, wherein step (D) comprises:

annealing each oxidized nanowire in an H_2 environment to passivate dangling bonds at the interface of an oxidized layer and a non-oxidized portion of each oxidized nanowire.

167. A method of fabricating nanowires having reduced surface scattering, comprising:

(A) selecting a semiconductor material;

(B) forming a plurality of nanowires from the selected semiconductor material; and

(C) doping each nanowire of the plurality of nanowires so that each nanowire comprises a core-shell structure, wherein the shell is a doped outer layer of each nanowire surrounding a respective core;

wherein step (C) comprises:

causing carriers of each nanowire to be substantially confined to the core during operation.

168. The method of claim 167, wherein step (C) comprises:

selecting a dopant material for the doped outer layer of each nanowire such that the doped outer layer would have a higher energy level relative to an energy level of the respective core; and

doping each nanowire of the plurality of nanowires using the selected dopant material.

169. The method of claim 167, wherein said doping step comprises:

selecting a dopant material for the doped outer layer so that a lattice structure of the doped outer layer substantially matches a lattice structure of the core; and

doping each nanowire of the plurality of nanowires using the selected dopant material.

170. A semiconductor device having reduced surface scattering, comprising:

a plurality of conducting nanowires, wherein each nanowire comprises

a core that comprises a semiconductor material, and

a shell that surrounds the respective core, wherein said shell comprises said semiconductor material doped with a dopant material;

wherein said doped semiconductor material causes carriers of said each nanowire to be substantially confined to the respective said core during operation.

171. The semiconductor device of claim 170, wherein said dopant material causes said shell to have a higher energy level relative to an energy level of said respective core.

172. The method of claim 170, wherein said dopant material causes said shell to have a lattice structure that sufficiently matches a lattice structure of said respective core to cause said carriers of said each nanowire to be substantially confined to said respective core during operation.